Detection of OPC Conflict Edges through MEEF Analysis

Li-Fu Chang[1], Chang-IL Choi[1], Guojie Cheng[2], Abhishek Vikram[2], Gary Zhang[2] and Bo Su[3]

[1]Semiconductor Manufacturing International Corporation,
18 Zhangjiang Road, Pudong New Area, Shanghai 201203, China
[2]Anchor Semiconductor, 666 Beijing Road East, Shanghai, China
[3]Anchor Semiconductor, 5403 Betsy Ross Drive, Santa Clara, CA 95054 USA

ABSTRACT

Semiconductor foundries at 65nm, 45nm, and more advanced technologies have witnessed high-yield mass production to be intimately correlated to the practice of adaptive DFM (Design for Manufacturability). With device performance variance easily exceeding 50% for 65nm and below, adaptive actions by designers, like modifying layouts to relieve potential DFM risks, is found to be a very efficient approach to high yield manufacturing. Rigorous MEEF estimation based methods have been proposed to achieve adaptive DFM by predicting mask writing variations at early stages (cell/block levels) of designs.

In a recent study, we discovered that by adding MEEF check in simulation contour based OPC verification flow, and by comparing MEEF changes of pre and post OPC hotspots, it is possible to separate OPC issues from design issues, in particular, for hotspot patterns with tight spaces with little room for any biases. We found that hotspot patterns with tight spaces usually create OPC conflict edges—correcting one edge will result in increasing MEEF at other edge, or vice versa. While advancement in OPC technology continues to improve MEEF performance, nevertheless OPC-conflicting edges almost always exist in designs at 65nm and below.

In this paper, we first demonstrate the existence of OPC conflict edge hotspots using MEEF analysis, in particular, the MEEF increase after OPC on those edges actually has smaller process window than pre-OPC ones. In certain cases, design modification is necessary to correct such OPC conflicting edges. Based on the finding, we propose a practical methodology of detecting design related OPC edge conflicting hotspots in a pattern centric software-based DFM (design for manufacturability) flow. The methodology is aiming to detect patterns containing such conflicting edges, and pursuing layout actions on the design side to eliminate this issue. We will validate the flow using a real design case. In addition, the OPC edge conflicting hotspots can be clipped and saved in a designated pattern library as hotspot templates, and incoming designs can be quickly screened using exact and similar pattern search with those saved templates in the library.

Key words: Design for manufacturability, Optical proximity correction, Mask error enhancement factor

INTRODUCTION

Mask error enhancement factor (MEEF) plays an important role in pattern transfer from design to silicon wafer. Cost of mask making has been increasing drastically with shrinking design size due to complex RET techniques employed to maintain small feature printability. Simulation based OPC verification has been widely adopted in OPC flow since 90nm technology node. As industry progresses towards 45nm and 32nm nodes and below, CD error and edge placement error (EPE) based checking at the best exposure conditions has shown its limitations in detecting marginal hotspots, which only become problematic with process variations. This makes it more important to analyze the chip in the design stage and find out and fix potential weak patterns to increase the manufacturability of the chip. Several studies have been done in the past to ascertain the impact of MEEF in chip manufacturing using simple line/space features [1, 2]. There are existing tools to offer full chip MEEF analysis [3] in addition to Post-OPC verification in the design stage. This can be time consuming and in addition generate overwhelming amount of data. In this paper we present a Design for Manufacturability (DFM) methodology to do MEEF analysis of hotspots. The purpose is to pick out the hotspots most sensitive to process variations.

It is known that high MEEF features restrict the full chip Process Window (PW) [4], such that they cannot be ignored in the lithographic process. When proximity effect strengthens around complex and size-minimizing features, the risk of printing failure, described by MEEF index, increases. Post-OPC MEEF indices then become worse than pre-OPC in such conflicting edges, breaking the fundamental principle that 'OPC improves printability'. While advancement in OPC technology continues to improve MEEF, OPC-conflicting edges almost always exist in designs at 65nm and below. For Foundry companies, it is critical to ensure lithographic friendly designs from their customers, in addition to DRC clean. Post OPC verification is the last simulation based check before mask making. However, separation of OPC correctable hotspots and non-OPC correctable hotspots is needed, since the responsibility of fixing those hotspots normally falls into two different companies. In this paper, we propose a new methodology to resolve the issue from a DFM perspective. Using a pattern centric software [5], we will demonstrate that in a given defect list, in this case from post-OPC verification, by comparing MEEF changes of pre and post OPC edges of hotspots, it is possible to separate OPC issues from design issues, in particular, for hotspot patterns with tight spaces with little room for any biases. Design features with varying Critical Dimension (CD) sizes have been studied to ascertain the impact on MEEF.

APPLICATION FLOW

We demonstrate the MEEF analysis for the hotspots detected in full chip post-OPC verification. In principle defect list from any design based check can be used to analyze MEEF sensitivity. The idea is to detect OPC conflict edges and filter the most sensitive hotspots out. The software used has integrated MEEF calculation capability for the hotspots and can save the MEEF values with the defect list. Since the MEEF calculation is done on defect clips instead of full chip design hence this approach is much faster. Using interactive histogram GUI, defects with high MEEF ratio (at Post-OPC edge/ at Pre-OPC edge) can be filtered and studied in detail. Here the same lithography model is used as in the Post-OPC verification stage, without any extra burden of data preparation. The filtered defect pattern clips can be saved into a pattern library and continuously accumulate from same device types for future use. The application flow is

depicted in Figure 1.

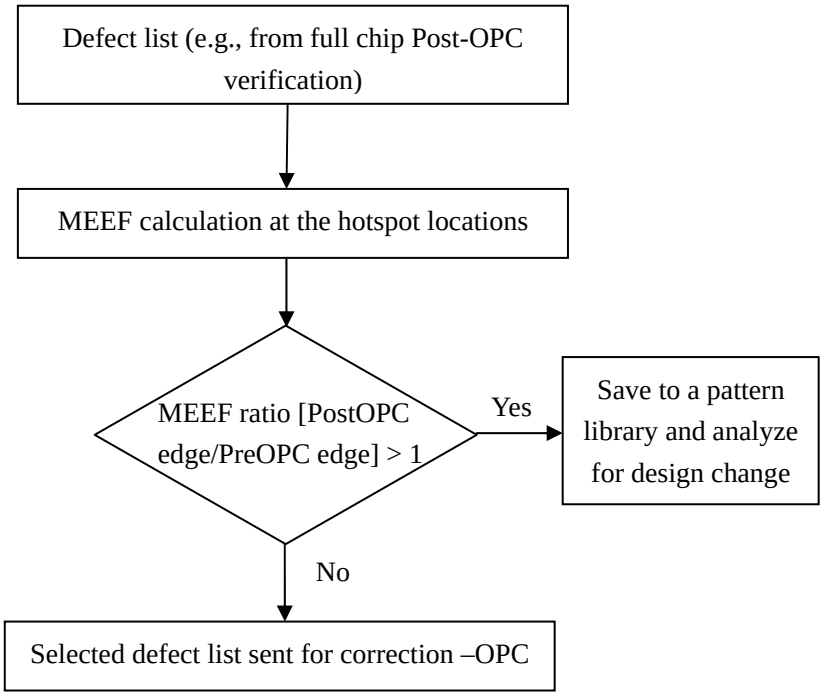

Figure 1: DFM flow for MEEF ratio analysis at hotspot locations

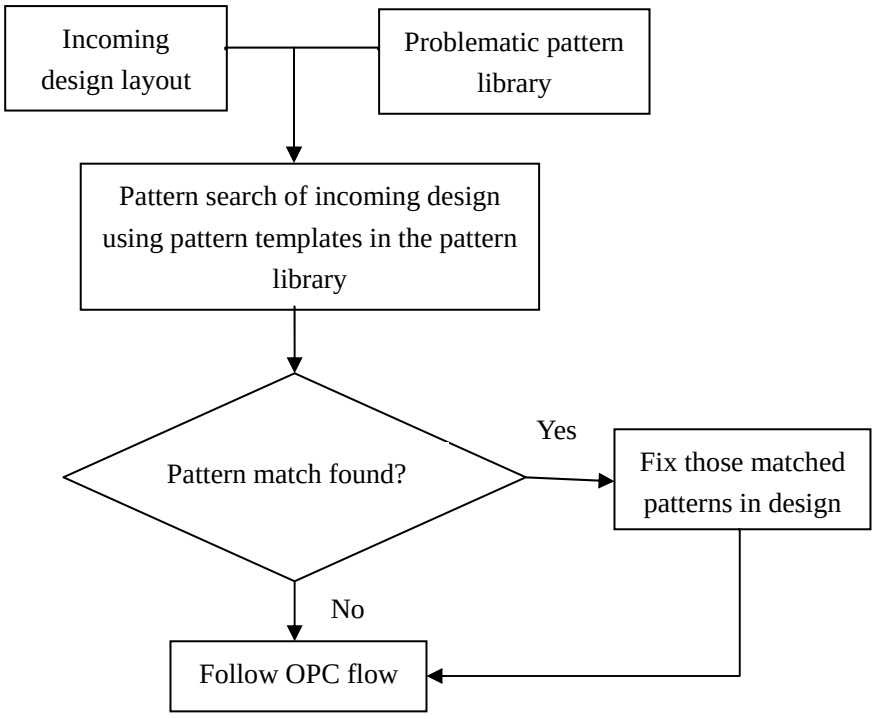

Figure 2: DFM flow using pattern search from incoming design screening.

After the buildup of problematic patterns in the pattern library as in Figure 1, an incoming design can be quick screened using pattern search method, instead of full chip simulation, even before OPC step. The application flow of such quick screening is shown in Figure 2. The advantage of this flow is to detect OPC conflict edge patterns through pattern match even before OPC step, to avoid lengthy and time-consuming OPC and OPC verifications. The condition of such flow is the existence of problematic pattern templates in a pattern library.

In the following sections, we present the detailed analysis results using a couple of test structures designed from real production cases as examples to demonstrate the existence of OPC conflict edge patterns and possible fixes of those conflict edges. The test structures are taken from the OPC conflict edge pattern library build on two critical layers: Metal 1 and Poly gate layers.

RESULTS AND DISCUSSIONS

In general, OPC improves design layout MEEF/NILS in the pattern transfer process (lithography) from design to wafer, thus its printability. However, in recent MEEF analysis of post OPC hotspot patterns, we found that is not always the case. Here we present two examples from two different layers to illustrate such exceptions.

Real case hotspot patterns from post-OPC verification results of a logic device of 65nm technology node (Metal-1 and Poly layers) with high MEEF have been used to design hotspot structures. Furthermore, similar structures with varying CD of the potential OPC conflict edges to demonstrate the variation in MEEF are also created. Production recipe is used in OPC decoration on those test patterns to ensure production OPC quality.

EXAMPLE OF METAL-1 PATTERN:

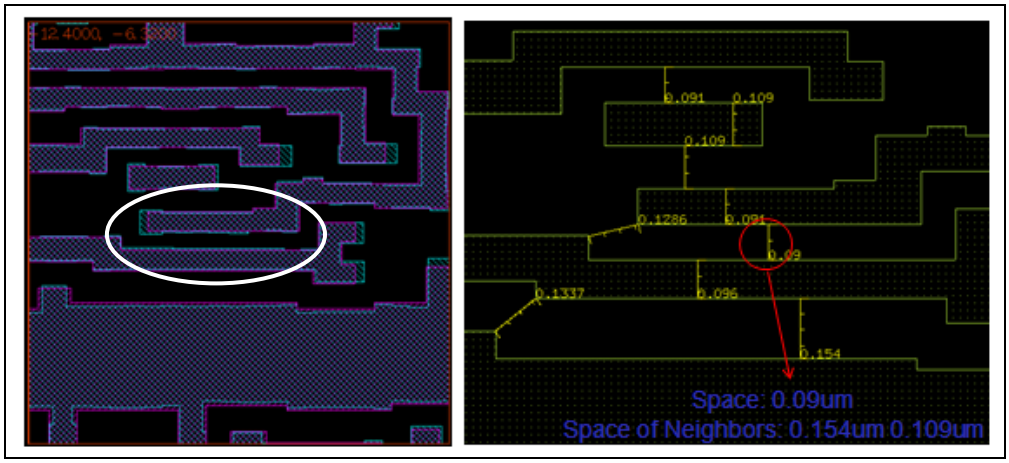

Figure 3: Test pattern from Metal-1 layer- tight space (90nm) between two adjacent lines resulting in bridge type defect in post OPC verification.

Figure 3 depicts a bridging hotspot of a constrained space in the neighborhood of a large metal structure,

which is difficult for doing effective OPC. The MEEF analysis shows (in Figure 4) that the MEEF of either edge of the adjacent lines are getting worse after OPC, as compared to pre-OPC.

The largest MEEF at the edges in the target layer is 3.7 which should ideally reduce after OPC but in fact it increases to 4.7, thereby resulting as OPC conflicting edges. This is because of the tight space (90nm) between the adjacent lines. Given the fact that the MEEF value of the hotspot at pre-OPC is already too high, the normal remedy in this case is to modify the design.

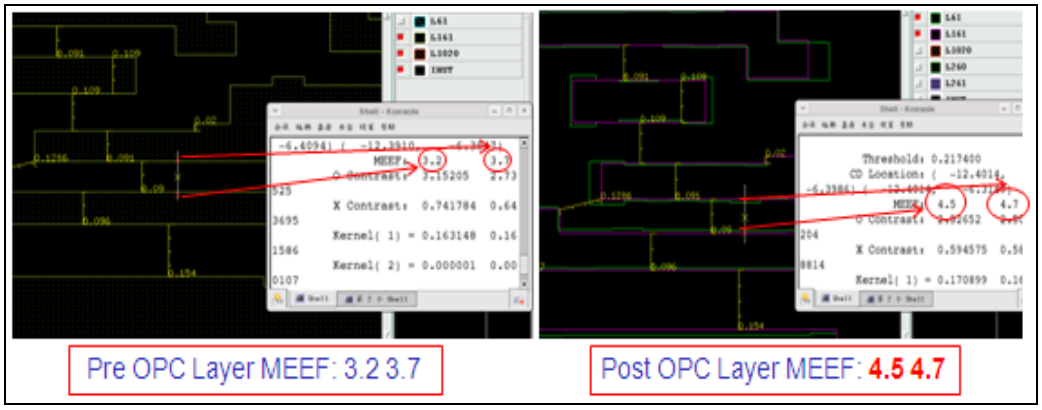

Figure 4: MEEF measurement on either edge of the hotspot location between the lines. The layout on the left shows measurement on pre-OPC structure and the one on right shows measurement on post-OPC structure

Design correction is applied to this hotspot structure by increasing the space to 110nm between the two adjacent lines through shifting each line 10nm on both sides, and remove jogs in the target layer to make the OPC easier. In this case, such moves are possible due to larger spaces in the neighborhood.

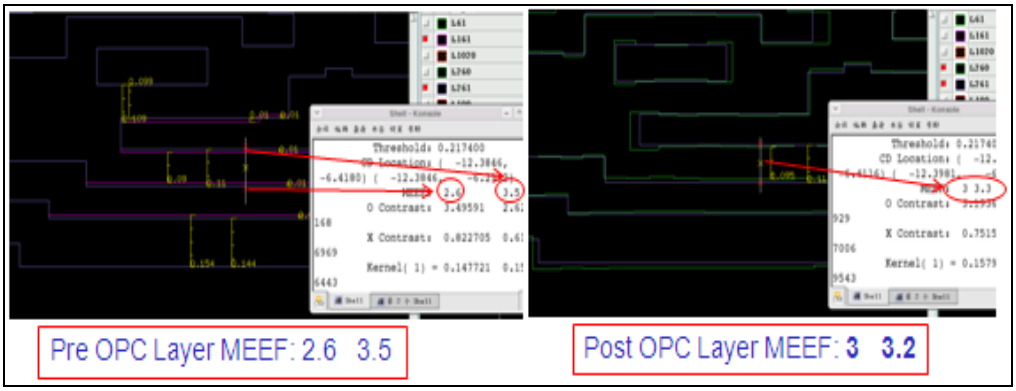

Figure 5: After design correction- MEEF measurement on either edge of the hotspot location between the lines. The layout on the left shows measurement on pre-OPC structure and the one on right shows measurement on re-optimized OPC structure

As a result of the layout modification, the largest MEEF on the re-optimized OPC edge becomes 3.2, reduced from the original value of 4.7, and also the MEEF ratio [post OPC edge / pre OPC edge] reduces from 4.7/3.7=1.3 to 3.2/3.5=0.9.

The MEEF variation as a function of the change in spaceCD between the two conflict edges of the hotspot pattern is summarized in Figure 6. The graph indicates that when the spaceCD becomes smaller than about 100nm, the OPC conflict edges appear. And such restriction in the space for this kind of hotspot patterns can become DFM guidelines for future lithography friendly designs in Metal-1 layer.

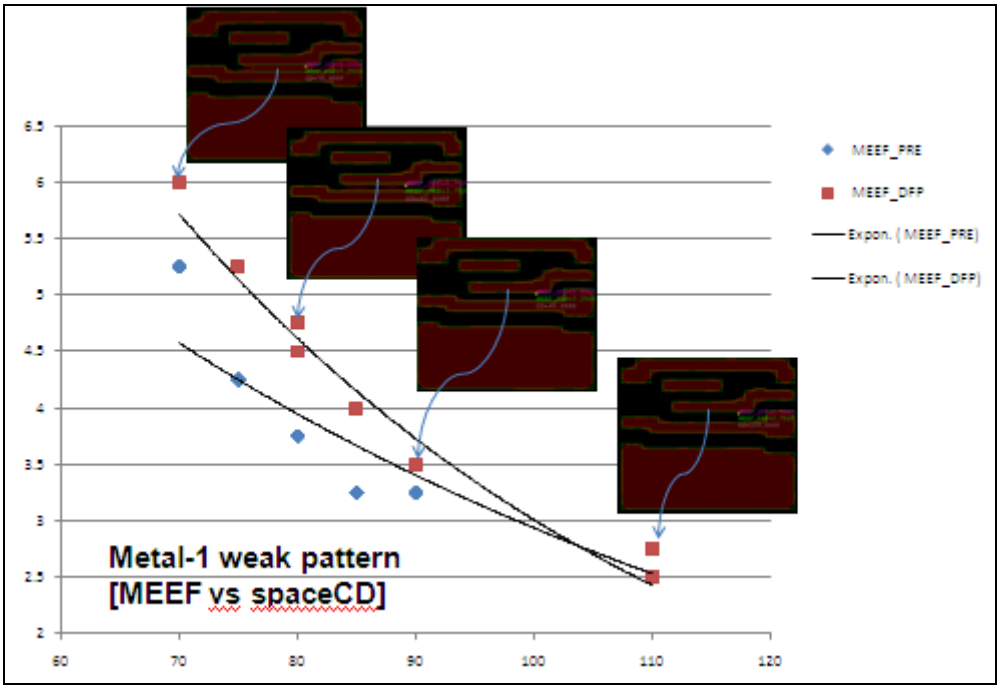

Figure 6: Change in MEEF at the pre and post OPC edges, also shown is the contour pattern for different spaceCD values.

EXAMPLE OF POLY GATE PATTERN:

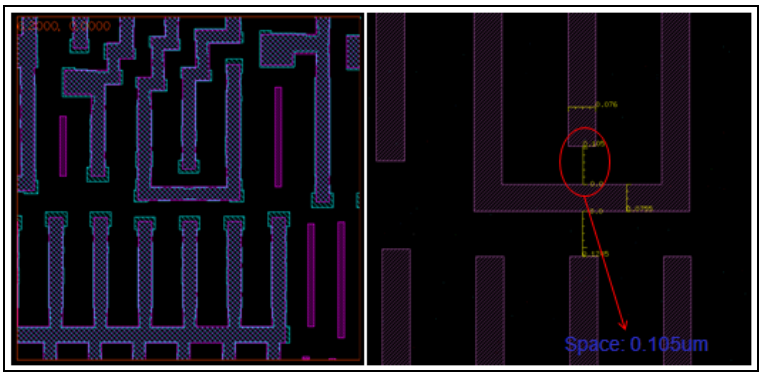

Figure 7: Test pattern from Poly layer- a center line (75nm) between two line ends with tight space (105nm), resulting in line end pullback

The test structure in Figure 7 depicts a tight space between a center line and two line-end poly structure,

which is difficult for doing effective OPC. The MEEF analysis results on the line end edge and the center line edge are shown in Figure 8. The MEEF measurement at the edge of the line end in target layer is 4.8, owing to which it has a large pullback 51.9nm; and OPC reduces the MEEF value to 3.5 for this edge. At the edge of the center line, however, the MEEF of the post-OPC edge increases drastically to 4.5, almost double that at the pre-OPC edge (2.3).

Unlike the previous example in Metal-1 layer, the two edges involved in this hotspot pattern shows MEEF improvement for the line end edge and MEEF degradation for the center line edge due to OPC. Without prioritizing which edge is more important here, any attempt to improve MEEF on one edge will result MEEF degradation on the other.

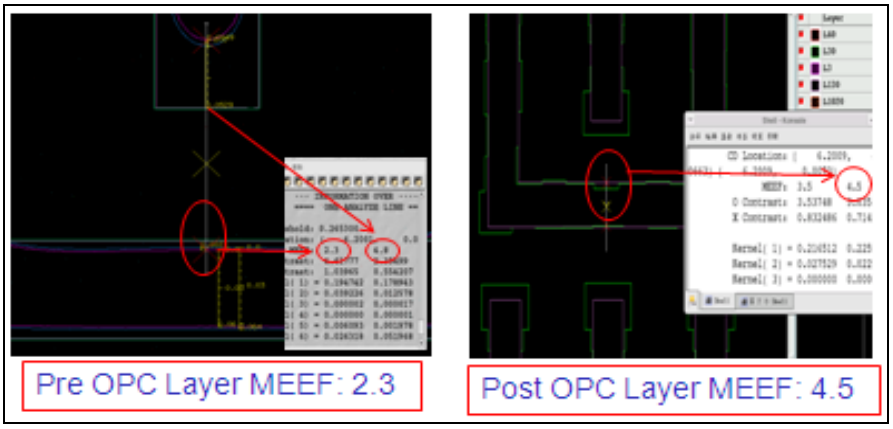

Figure 8: Test MEEF measurement on either edge of the hotspot location between the lines. The layout on the left shows measurement on pre-OPC structure and the one on right shows measurement on post-OPC structure

Design correction is applied to this hotspot structure—the line end is shifted back by 20nm. This design change releases space between the line end and the center line, and the OPC is re-optimized for the center line as shown in Figure 9.

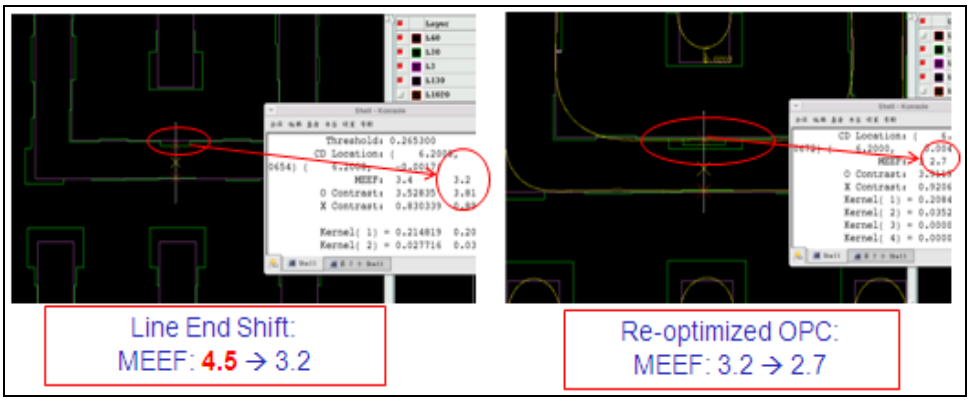

Figure 9: MEEF values on the edge of the center line after design correction. The layout on the left shows MEEF on post-OPC center line structure with line end shifted back by 20nm; and the one on right shows MEEF on re-optimized OPC center line structure

As a result the MEEF on the center line re-optimized OPC edge becomes 2.7, reduces from the original structure 4.5, and also the MEEF ratio [post OPC edge / pre OPC edge] reduces from 4.5/2.3=1.9 to 2.7/2.2=1.2, still above 1. Further design modification is needed.

The MEEF variation as a function of the change in spaceCD between line end to the center line is summarized in Figure 10. The chart shows near linear increase of MEEF, as the space between the line end and the center line decreases; and the space CD should be around 150nm for such line end and center line configuration to avoid OPC edge conflict, which can become a DFM guideline for future lithography friendly designs.

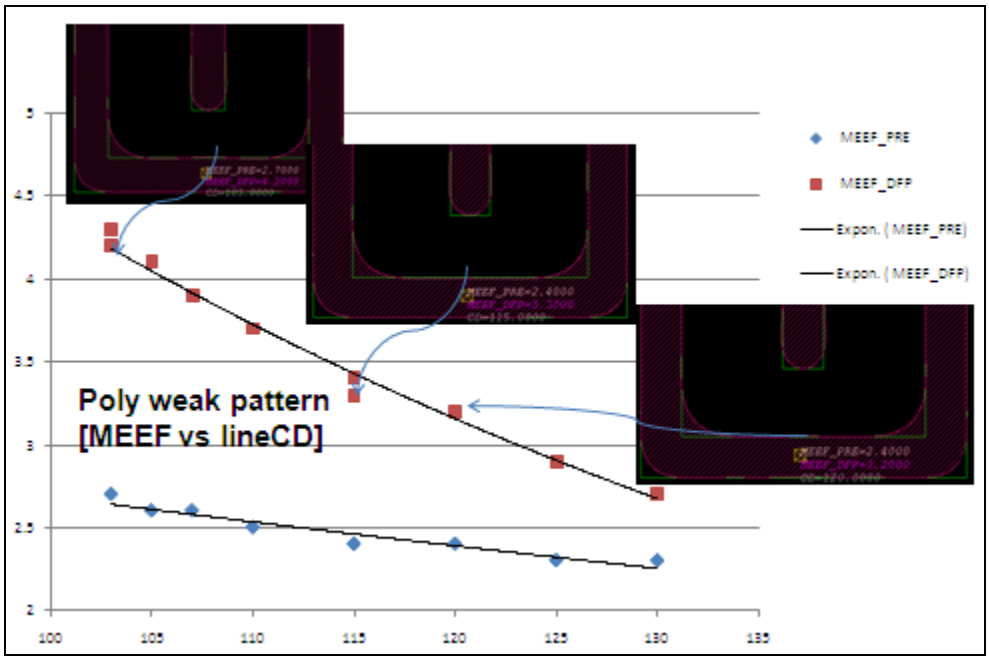

Figure 10: Change in MEEF of center line at the pre and post OPC edges, also shown is the contour pattern for different lineCD values

SUMMARY AND FUTURE WORK

Through MEEF analysis of post OPC verification hotspots, we find the existence of OPC conflict edges in critical layers of some customer designs; and OPC conflict edges can be detected by calculating MEEF at the pre and post OPC edges of hotspot patterns. A methodology of detecting OPC conflict edge patterns is proposed and verified on hotspot patterns from two critical layers. This methodology was applied in the real production case to filter the process sensitive hotspots from post-OPC verification result. With the accumulation of detected OPC conflict edge hotspot patterns in a pattern library, a quick screening is possible with pattern search technique for incoming designs to detect and fix OPC conflict edges even before OPC step.

The MEEF analysis methodology presented can be applied easily to other applications; for example,

multiple OPC scheme comparison, OPC hotspot fix verification, OPC hotspot monitoring and tracking in mask making process and etc. We will extend the flow to other applications in the future.

This MEEF analysis methodology can be utilized to do systematic study of a known hotspot and establish another way of building DFM Rules, in addition of existing methods. It will make the DFM rules more complete.

REFERENCES

[1] Franklin M. Schellenberg, Chris A. Mack, "MEEF in theory and Practice", Proc. SPIE **3873** (2003).

[2] Hye-Young Kang, et al, "Mask error enhancement factor variation with pattern density", Proc. SPIE **5992** (2005).

[3] Juhwan Kim, et al, "Full-chip level MEEF analysis using model based lithography verification", Proc. SPIE **5992** (2005).

[4] Guangming Xiao, et al, "Source optimization and mask design to minimize MEEF in low k1 lithography", Proc. SPIE **7028** (2008).

[5] Jae-Hyun Kang, et al, "Combination of rule and pattern based lithography unfriendly pattern detection in OPC flow", Proc. SPIE **7122** (2008).